CLAIMS

1. A booster circuit connecting and boosting basic charge pump cells disposed respectively at N stages, the booster circuit comprising:

said basic charge pump cells each including at least a first MISFET, a second MISFET, a third MISFET, and a first capacitor,

wherein a back gate of said first MISFET is connected to a first node and a source-drain path thereof is connected between a second node and a third node,

a back gate of said second MISFET is connected to said first node and a source-drain path thereof is connected between said first node and said second node, and

a back gate of said third MISFET is connected to said first node and a source-drain path thereof is connected between said first node and said third node.

2. The booster circuit according to claim 1,

wherein one end of said first capacitor is connected to said third node and a first clock with an amplitude of an operating voltage is inputted to the other end thereof, and

said third node is connected to a second node of said basic charge pump cell at a next stage.

3. The booster circuit according to claim 2,

wherein said basic charge pump cell further includes a fourth MISFET and a second capacitor,

one end of said second capacitor is connected to a gate of said first MISFET, and a second clock, having a voltage amplitude larger than that of a sum of said operating voltage and a threshold voltage of said first MISFET and being a reversed phase to said first clock, is inputted to the other end thereof, and

a back gate of said fourth MISFET is connected to said first node, an a source-drain path thereof is connected between said second node and the gate of said first MISFET, and a gate thereof is connected to said one end of said second capacitor configuring said basic charge pump cell at a preceding stage.

4. The booster circuit according to claim 2,

wherein said basic charge pump charge cell further includes a fourth MSFET and a second capacitor,

one end of said second capacitor is connected to a gate of said first MISFET, and a second clock, having a voltage amplitude larger than that of a sum of said operating voltage and a threshold voltage of said first MISFET and being a same phase as that of said first clock, is inputted to the other end thereof, and

a source-drain path of said fourth MISFET is connected between said third node and the gate of said first MISFET, and a gate thereof is connected said one end

of said second capacitor configuring said basic charge pump cell at a preceding stage.

5. The booster circuit according to claim 1,

wherein said first, second, third, fourth MISFETs are n-type MISFETs, and

a voltage is boosted on a positive side.

6. The booster circuit according to claim 1,

wherein said first, second, third, and fourth MISFETs are p-type MISFETs, and

a voltage is boosted on a negative side.

7. The booster circuit according to claim 1,

wherein said first, second, third, and fourth MISFETs are n-type MISFETs, and

a voltage is boosted on a negative side.

8. The booster circuit according to claim 1,

wherein said first, second, third, and fourth MISFETs are p-type MISFETs, and

a voltage is boosted on a positive side.

9. The booster circuit according to claim 3, further comprising:

a twice boosted clock generating circuit for generating a clock of a voltage twice as much as said

operating voltage, and

wherein said twice boosted clock generating circuit generates said second clock.

10. The booster circuit according to claim 3,

wherein said first clock inputted to said basic charge pump cells at odd-numbered stages and said first clock inputted to them at even-numbered stages are opposite in phase, and

said second clock inputted to said basic charge pump cells at the odd-numbered stages and said second clock inputted to them at the even-numbered stages are opposite in phase.

11. A booster circuit connecting and boosting basic charge pump cells disposed respectively at N stages, the booster circuit comprising:

said basic charge pump cells each including an n-type transfer MISFET, and a connection circuit for connecting a drain or source of said transfer MISFET, whichever is lower in potential, said transfer MISFET, and a back gate thereof.

12. The booster circuit according to claim 11,

wherein said connection circuit is configured by a first body controlled MISFET and a second body controlled MISFET, and

one of said first and second body controlled MISFETs

is conducted and the drain or source of said transfer MISFET, whichever is lower in potential, and the back gate of said transfer MISFET are connected.

13. A booster circuit connecting and boosting basic charge pump cells disposed respectively at N stages, the booster circuit comprising:

said basic charge pump cells each including a p-type transfer MISFET, and a connection circuit for connecting a drain or source of said transfer MISFET, whichever is higher in potential, said transfer MISFET, and a back gate thereof.

14. The booster circuit according to claim 13,

wherein said connection circuit is configured by a first body controlled MISFET and a second body controlled MISFET, and

one of said first and second body controlled MISFETs is conducted, and the drain or source of said transfer MISFET, whichever is higher in potential, and the back gate of said transfer MISFET are connected.

15. The booster circuit according to claim 1, further comprising:

a selection circuit for choosing which of plus and minus is boosted.

16. The booster circuit according to claim 15,

wherein said selection circuit is a circuit for connecting, to said operating voltage, a second node of one of said basic charge pump cells at a first stage and at a last stage and for connecting a third node of the other thereof to a ground potential.

17. The booster circuit according to claim 1, further comprising:

a serial-type charge pump,

wherein said serial-type charge pump outputs a second voltage from a first voltage outputted from said booster circuit.

18. A non-volatile memory executing at least one of reading, writing, and deletion in accordance with a voltage generated by the booster circuit according to claim 1.

19. An IC card including the non-volatile memory according to claim 18.